CLAIMS

What is claimed is:

1. A method for reading an MTJ in a ganged memory cell of an MRAM, comprising the steps of:

determining a first electrical value that is at least partially associated with a resistance of the ganged memory cell;

toggling the MTJ in the ganged memory cell of the MRAM;

determining a second electrical value that is at least partially associated with said resistance of the ganged memory cell after said toggling of the MTJ;

analyzing a difference between said first electrical value and said second electrical value.

2. The method for reading the MTJ in the ganged memory cell of the MRAM of Claim 1, wherein said first electrical value and said second electrical values are the net time-rate transference of charge through the ganged memory cell.

3. The method for reading the MTJ in the ganged memory cell of the MRAM of Claim 1, said method further comprising the steps of applying a known current to the ganged memory cell of the MRAM.

4. The method for reading the MTJ in the ganged memory cell of the MRAM of Claim 3, wherein said determining said first electrical value that is at least partially associated with said resistance of the ganged memory cell comprises measuring a first voltage across the ganged memory cell.

5. The method for reading the MTJ in the ganged memory cell of the MRAM of Claim 4, wherein said determining said second electrical value that is at least partially associated with said resistance of the ganged memory cell comprises measuring a second voltage across the ganged memory cell after said toggling the MTJ in the ganged memory cell of the MRAM.

6. The method for reading the MTJ in the ganged memory cell of the MRAM of Claim 4, wherein said analyzing a difference between said first electrical value and said second electrical value comprises determining a difference between said first voltage and said second voltage.

7. An MRAM, comprising:

a first memory cell having a first Magnetic Tunnel Junction (MTJ); and

a second memory cell having a second MTJ and at least partially forming a ganged memory cell with said first memory cell, wherein the first memory cell and the second memory cell are configured such that a read of the first MTJ comprises:

a determination of a first electrical value that is at least partially associated with a resistance of the ganged memory cell;

toggling the first MTJ of the first memory cell;

a determination of a second electrical value that is at least partially associated with said resistance of said ganged memory cell after toggling the first MTJ; and

an analysis of a difference between said first electrical value and said second electrical value.

8. The MRAM of Claim 7, wherein said first MTJ and said second MTJ comprise:

a first magnetic region;

a second magnetic region; and

a tunnel barrier region interposed between said first magnetic region and said second magnetic region.

9. The MRAM of Claim 8, wherein said first magnetic region comprises:

a first ferromagnetic layer;

a second ferromagnetic layer; and

a non-magnetic layer interposed between said first ferromagnetic layer and said second ferromagnetic layer.

10. The MRAM of Claim 8, wherein said second magnetic layer comprises:

an anti-ferromagnetic layer; and

a ferromagnetic layer adjacent to said anti-ferromagnetic layer.

11. The MRAM of Claim 7, wherein said first electrical value and said second electrical values are the net time-rate transference of charge through the ganged memory cell.

12. The MRAM of Claim 7, said read of the first MTJ further comprises application of a known current to the ganged memory cell of the MRAM.

13. The MRAM of Claim 12, wherein said determination of said first electrical value that is at least partially associated with said resistance of the ganged memory cell comprises measurement of a first voltage across the ganged memory cell.

14. The MRAM of Claim 12, wherein said determination of said second electrical value that is at least partially associated with said resistance of the ganged memory cell comprises measurement of a second voltage across the ganged memory cell after said toggle of the MTJ in the ganged memory cell of the MRAM.

15. The MRAM of Claim 14, wherein said analysis of a difference between said first electrical value and said second electrical value comprises a determination of a difference between said first voltage and said second voltage.

16. A Magnetoresitive Random Access Memory (MRAM), comprising:

a first bit line;

a first memory cell adjacent to said first bit line and consisting of a first Magnetic Tunnel Junction (MTJ);

a second memory cell at least partially forming a first ganged memory cell with said first memory cell and consisting of a second MTJ that is connected in series with said first memory cell; and

a first word line adjacent to said first memory cell and said second memory cell.

17. The MRAM of Claim 13, further comprising a first plurality of memory cells in addition to said first memory cell and said second memory cell, said plurality of memory cells at least partially forming said first ganged memory cell with said first memory cell and said second memory cell and said plurality of memory cells consisting of an MTJ that is connected in series with other MTJs of said first plurality of memory cells.

18. The MRAM of Claim 13, further comprising:

a third memory cell adjacent to said first bit line and consisting of a third MTJ;

a fourth memory cell at least partially forming a second ganged memory cell with said third memory cell and consisting of a fourth MTJ that is connected in series with said third memory cell; and

a second word line adjacent to said third memory cell and said fourth memory cell.

19. A Magnetoresitive Random Access Memory (MRAM), comprising:

a first word line;

a first ganged memory cell adjacent to a first word line, said first ganged memory cell having a first plurality of memory cells that include a Magnetic Tunnel Junction (MTJ), excluding an isolation device, and connected in series with other memory cells of said first ganged memory cell; and

a first bit line adjacent to at least one of said first plurality of memory cells of said first ganged memory cell.

20. The MRAM of Claim 19, wherein each of said first plurality of memory cells are connected in series with other memory cells of said first ganged memory cell and exclude parallel connections with other memory cells of said first ganged memory cell.

21. The MRAM of Claim 18, further comprising:

a second word line;

a second ganged memory cell adjacent to a second word line, said second ganged memory cell having a second plurality of memory cells that include said MTJ, excluding said isolation device, and connected in series with other memory cells of said second ganged memory cell; and

a second bit line adjacent to at least one of said second plurality of memory cells of said second ganged memory cell.

22. The MRAM of Claim 21, wherein each of said second plurality of memory cells are connected in series with other memory cells of said second ganged memory cell and exclude parallel connections with other memory cells of said second ganged memory cell.

23. The MRAM of Claim 17, wherein said first MTJ and said second MTJ comprise:

a first magnetic region;

a second magnetic region; and

a tunnel barrier region interposed between said first magnetic region and said second magnetic region.

24. The MRAM of Claim 18, wherein said first magnetic region comprises:

a first ferromagnetic layer;

a second ferromagnetic layer; and

a non-magnetic layer interposed between said first ferromagnetic layer and said second ferromagnetic layer.

25. The MRAM of Claim 18, wherein said second magnetic layer comprises:

an anti-ferromagnetic layer; and

a ferromagnetic layer adjacent to said anti-ferromagnetic layer.

26. A Magnetoresitive Random Access Memory (MRAM), comprising:

a first word line;

a first memory group adjacent to said first word line, said first memory group comprising a first memory cell coupled in parallel with a second memory cell and said first memory cell and said second memory cell consisting of a Magnetic Tunnel Junction (MTJ);

a second memory group coupled in series with said first memory group to form a first ganged memory cell, said second memory group comprising a third memory cell coupled in parallel with a fourth memory cell and said third memory cell and said fourth memory cell consisting of said MTJ; and

a first bit line adjacent to at least one of said first memory cell, said second memory cell, said third memory cell and said fourth memory cell.

27. The MRAM of Claim 26, said first memory group further comprises:

a fifth memory cell coupled in series with said first memory cell and coupled in parallel with said second memory cell; and

a sixth memory cell coupled in series with said second memory cell and coupled in parallel with said first memory cell.

28. The MRAM of Claim 26, wherein said MTJ comprises:

a first magnetic region;

a second magnetic region; and

a tunnel barrier region interposed between said first magnetic region and said second magnetic region.

29. The MRAM of Claim 28, wherein said first magnetic region comprises:

a first ferromagnetic layer;

a second ferromagnetic layer; and

a non-magnetic layer interposed between said first ferromagnetic layer and said second ferromagnetic layer.

30. The MRAM of Claim 28, wherein said second magnetic layer comprises:

an anti-ferromagnetic layer; and

a ferromagnetic layer adjacent to said anti-ferromagnetic layer.

31. The MRAM of Claim 26, further comprising a third memory group coupled in series with said first memory group and said second memory group to form said first ganged memory cell, said third memory group comprising a first plurality of memory cells coupled in parallel and each of said second plurality of memory cells consisting of said MTJ.

32. A Magnetoresitive Random Access Memory (MRAM), comprising:

a first word line;

a first memory group adjacent to said first word line, said first memory group comprising a first memory cell coupled in series with a second memory cell and said first memory cell and said second memory cell consisting of a Magnetic Tunnel Junction (MTJ);

a second memory group coupled in parallel with said first memory group to form a first ganged memory cell, said second memory group comprising a third memory cell coupled in series with a fourth memory cell and said third memory cell and said fourth memory cell consisting of said MTJ; and

a first bit line adjacent to at least one of said first memory cell, said second memory cell, said third memory cell and said fourth memory cell.

33. The MRAM of Claim 32, said first memory group further comprises:

a fifth memory cell coupled in series with said first memory cell and said second memory cell; and

a sixth memory cell coupled in series with said third memory cell and said fourth memory cell.

34. The MRAM of Claim 32, wherein said MTJ comprises:

a first magnetic region;

a second magnetic region; and

a tunnel barrier region interposed between said first magnetic region and said second magnetic region.

35. The MRAM of Claim 34, wherein said first magnetic region comprises:

a first ferromagnetic layer;

a second ferromagnetic layer; and

a non-magnetic layer interposed between said first ferromagnetic layer and said second ferromagnetic layer.

36. The MRAM of Claim 34, wherein said second magnetic layer comprises:

an anti-ferromagnetic layer; and

a ferromagnetic layer adjacent to said anti-ferromagnetic layer.